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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/508,795	09/21/2004	Tatsuo Tsujita	Q83757	3903

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EXAMINER	
YOUNG, BRIAN K	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 02/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/508,795	TSUJITA, TATSUO	
	Examiner	Art Unit	
	Brian Young	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *16-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16,19 and 24* is/are rejected.

7)☒ Claim(s) *17,18,20-23 and 25-30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 September 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/21/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 16,19 and 24 are rejected under 35 U.S.C. 102(e) as being anticipated by Eklund. Eklund discloses (fig.4) a circuit comprising: a plurality of analog/digital converting circuits (13) operated in parallel for sequentially converting an analog signal to a digital signal; and a multi-phase clock signal generating circuit (15) for generating multi-phase clock signals to be used for periodically operating said plurality of analog/digital converting circuits in a certain order. Eklund further discloses (fig.6) a control circuit (Random Number Generator) for controlling said clock signal circuit to change at least one of a period and an order of operating said plurality of analog/digital converting circuits. Eklund recites that the device is useful in "communications" systems (col.1, lns.15-17), which, could include images.

Eklund recites (col.4,ln.66-col.5ln.42):

"The operation of the time control unit 15 is the following. When a new clocking pulse is issued by the clock signal generator 23, the clock signal passes through the output 1:5 selector 37 to the selected j:th output thereof and to the sample and hold circuit 11.sub.j for the selected channel, This starts the conversion process in the j:th channel. At the same time the clocking pulse moves two selectors 27, 29 at the input and output sides of the

registers 25 for active channels to the next register 25.sub.i in a cyclical order. Then that register 25.sub.i is selected by the two selectors which has finished its conversion time a short time period before the clocking pulse. The channel number stored in that register 25.sub.i is fed to the input of the 2:1 selector 33, on the other input of which is provided the number of the idling channel from the register 31. The position of the 2:1 selector 33 is controlled by the output signal of the choice generator 21, which when receiving the clocking pulse outputs a new bit. The chosen one of the numbers of the ready channel and the idling channel is through the delay circuit 35 provided to the output selector 37 and changes the position thereof to the correct output. The number of the ready channel has then been copied to the intermediate register 39. As controlled by the control units 41, 43 responsive to the output bit of the choice generator 21, only for a bit signifying a logical "one", the channel number stored in the register 31 for the idling channel is copied to the register 25.sub.i as selected by the selector 27 at the input side of the active channel registers 25 and thereafter the channel number stored in the intermediate register 39 is copied to the register 31 for the idling channel.

As mentioned above, a parallel ADC device has systematic errors like e.g. jitter and gain errors, i.e. the individual ADCs have characteristics differing from each other, e.g. the gain being different for the individual

ADCs. The systematic errors or differences cause undesired tones in the output, combined signal of the composite ADC device. These tones restrict the dynamic range of the parallel ADC device. When the next channel to make a conversion is selected in a random way or in some systematic way having a sufficient period among at least two individual ADCs, the pattern of undesired tones which can be called a signal distortion is transformed to noise. The total energy of the error is still approximately the same but the characteristics thereof have been totally changed. The error is now distributed in the frequency domain and is not collected at some peaks. In some cases the noise can be lower than the quantification noise and has then practically disappeared."

3. Claims 17,18,20-23, and 25-30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Reyneri disclose a circuit which includes an input terminal coupled to receive an analog input signal, a multiple number of sample-and-hold circuits and a multiple number of

analog-to-digital (A/D) converters. The input terminal of each of the sample-and-hold circuits is coupled to receive the analog input signal. Each of the A/D converters has an input terminal and an output terminal, where the

input terminal is coupled to an output terminal of a corresponding one of the sample-and-hold circuits. In operation, the sample-and-hold circuits sample the analog input signal sequentially and store a multiple number of analog samples at each of the sample-and-hold circuits. The A/D converters convert the analog samples in parallel to generate digital values at the output terminals of each of the A/D converters representative of each of the analog samples. In one embodiment, the A/D converters are implemented based on a multi-channel bit-serial (MCBS) analog-to-digital conversion scheme.

Nairn disclose a parallel analog-to-digital converter systems provided in which converters are temporally interleaved. In particular, converters are partitioned into at least two converter groups which are assigned different respective group converter periods that are multiples of the system periods. With converters in each of the converter groups, respective samples are processed over that group's respective group converter period and the group converter periods of all converters are temporally shifted to process each of the samples with at least one of the converters. System spurious signals are thus reduced and, in another system embodiment, the reduced spurious lines are converted into the system's noise level by detecting instances when available converters that belong to different converter groups are available to process an upcoming one of the samples and, in at least a chosen one of the instances, exchanging the available converters between their different converter groups to

thereby alter which processes the upcoming sample and which processes a subsequent sample. All converters continue to process respective samples.

Siferd discloses a bandpass analog to digital converter includes M single channel delta modulators having N-bit quantizer outputs arranged in a parallel configuration and operated at a predetermined sample frequency (f.sub.s). The modulator outputs are time interleaved and digitally combined in a manner that provides performance characteristics comparable to a modulator with a sample frequency of Mf.sub.s. Thus, bandpass center frequencies that are much higher than conventional single channel architectures are achievable. Single channel first order modulator bandpass center frequencies are restricted to f.sub.c =f.sub.s /4. However, a range of center frequencies approaching Mf.sub.s /2 is supported. This increased frequency capability is obtained while maintaining the delta sigma noise shaping near the higher bandpass center frequencies to reduce the effects of quantization noise. This results in a high signal to noise ratio with a corresponding high resolution at the much higher center frequencies.

Gustavsson discloses ADC (switched capacitor analog-to-digital converter) includes a passive sampling technique controlled by a global clock phase to reduce the influence of the sampling phase skew. Since it does not require operational amplifiers for sampling, it is very suitable for high speed applications, and

yet it can reduce the sampling-phase-skew-related distortion by 20-40 dB in a high speed, parallel SC ADC.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian Young whose telephone number is 571-272-1816. The examiner can normally be reached on Mon-Fri 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brian Young
Primary Examiner
Art Unit 2819

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